What is claimed is:

1. A Single Instruction Multiple Data (SIMD) digital signal processor, comprising:

an on-chip program memory for storing an instruction data of a program;

a plurality of main instruction decoders for decoding the instruction data and outputting a decoded signal;

an on-chip data memory for storing data; and

a plurality of arithmetic units for calculating the data according to the decoding signal.

2. The processor of claim 1, wherein the plurality of instruction decoders comprise:

a main instruction decoder for decoding an instruction data performed in case the above condition is satisfied, according to the condition of the conditional branch; and

a sub instruction decoder for decoding an instruction data performed in case the above condition is not satisfied.

3. The processor of claim 1, wherein the plurality of arithmetic units independently or identically calculate according to the characteristic of the instruction data.

4. A Single Instruction Multiple Data (SIMD) digital signal processor, comprising:

an on-chip program memory for storing an instruction data of a program;

a main instruction decoder for decoding the instruction data and outputting a decoded signal;

a sub instruction decoder for decoding a received instruction data in case of an instruction mode related to a conditional branch;

an on-chip data memory for storing the data;

a main arithmetic unit for calculating the data according to the decoded signal of the main instruction decoder; and

a sub arithmetic unit for calculating the data identically as the main arithmetic unit according to the decoded signal of the main instruction decoder or calculating the data according to the decoded signal of the sub instruction decoder.

5. An arithmetic method for a Single Instruction Multiple Data (SIMD) digital signal processor, comprising the steps of:

decoding an instruction data fetched from an on-chip program memory in the main instruction decoder; and

calculating according to the characteristic of the instruction data after determining the characteristic of the decoded instruction data.

6. The method of claim 5, further comprising the steps of:

transmitting the decoded instruction data into a main arithmetic unit in case the characteristic of the instruction data corresponds to the normal instruction data in the result of the above determination; and

calculating in the main arithmetic unit, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data

memory.

7. The method of claim 5, further comprising the steps of:

transmitting the decoded instruction data into a main arithmetic unit and sub arithmetic unit in case the characteristic of the instruction data corresponds to the SIMD instruction data in the result of the above determination; and

calculating in the main arithmetic unit and sub arithmetic unit respectively, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data memory.

8. The method of claim 7, wherein the calculations in the main arithmetic unit and sub arithmetic unit are identical.

9. The method of claim 5, further comprising the steps of:

calculating according to the decoded instruction data in case the characteristic of the instruction data corresponds to a predetermined conditional branch in the result of the above determination; and

respectively decoding the instruction data by fetching simultaneously the instruction data which will be performed in case the condition of the conditional branch is satisfied and in case not satisfied and calculating according to the decoded instruction data.

10. The method of claim 9, wherein the step of calculating comprises:

decoding the instruction data by fetching the instruction data which will be performed in case the condition of the conditional branch is satisfied and decoding

in the sub instruction decoder by fetching the instruction data which will be performed in case the condition of the conditional branch, at the same time; and

calculating the in the main arithmetic unit and sub arithmetic unit respectively, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data memory.

11. The method of claim 10, further comprising a step of:

maintaining the state information of the main instruction decoder and main arithmetic unit if the condition that the condition is satisfied, after determining the condition of the conditional branch, and deleting the state information of the sub instruction decoder and sub arithmetic unit.

12. The method of claim 10, further comprising a step of:

deleting the state information of the main instruction decoder and main arithmetic unit if the condition that the condition is not satisfied, after determining the condition of the conditional branch, and replacing the information with the state information of the sub instruction decoder and sub arithmetic unit.

13. An arithmetic method for a Single Instruction Multiple Data (SIMD) digital signal processor, comprising the steps of:

determining the characteristic of the decoded instruction data by decoding the instruction data fetched from the on-chip program memory in the main instruction decoder;

transmitting the decoded instruction data into the main arithmetic unit in case the characteristic of the instruction data corresponds to a predetermined

conditional branch in the result of the above determination;

calculating the condition of the conditional branch in the main arithmetic unit according to the decoded instruction data by reading the data necessary for calculating from an on-chip data memory;

decoding the instruction data respectively in the main instruction decoder and sub instruction decoder by simultaneously fetching the instruction data which will be performed in case the condition of the conditional branch is satisfied and in case not satisfied and then calculating respectively in the main arithmetic unit and sub arithmetic unit according to the decoded instruction data; and

deleting one among the state information of the main instruction decoder and main arithmetic unit and the state information of the sub instruction decoder and sub arithmetic unit, according to the satisfaction of the condition, when the condition of the conditional branch is determined.

14. The method of claim 13, further comprising the steps of:

transmitting the decoded instruction data into the main arithmetic unit in case the characteristic of the instruction data corresponds to a normal instruction data in the result of the above determination

calculating the condition of the conditional branch in the main arithmetic unit, according to the decoded instruction data by reading the data necessary for calculating from the on-chip data memory.

15. The method of claim 13, further comprising the steps of:

transmitting the decoded instruction data into a main arithmetic unit and sub arithmetic unit in case the characteristic of the instruction data corresponds to

the SIMD instruction data in the result of the above determination; and

calculating in the main arithmetic unit and sub arithmetic unit respectively, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data memory.

16. The method of claim 13, wherein the condition is satisfied, the state information of the main instruction decoder and main arithmetic unit is left as it is and the state information of the sub instruction decoder and sub arithmetic unit is deleted.

17. The method of claim 13, wherein the condition is not satisfied, the state information of the state information of the main instruction decoder and main arithmetic unit is deleted and the information is replaced by the state information of the sub instruction decoder and sub arithmetic unit.